A SELF-CASCODE BASED SUBTHRESHOLD POSITIVE FEEDBACK ADIABATIC LOGIC FOR ULTRA LOW POWER APPLICATIONS

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Abstract- The self-cascode positive feedback adiabatic logic (SC-PFAL) is reported as a promising candidate for low power applications. In this paper concept of self cascoding of transistor is applied to adiabatic logic working in sub-threshold region to enhance the energy efficiency of the gates. A library of gates based on proposed logic is designed and simulated using 70nm technology model file available from predictive technologies. Application of self cascode to adiabatic logic gates is explored for the first time in the literature. The spice simulation results illustrate these logic cells have significant improvement in terms of power consumption over their original PFAL and other adiabatic logic counterpart when operated at low frequency.

Keywords- Adiabatic logic, Self-cascode, PFAL, Ultra-low power

1. INTRODUCTION

Low power consumption is a mandatory prerequisite for many modern day applications like body implanted biomedical systems, battery driven devices, devices powered by harvesting energy from environment etc. New technologies like IOT demands for ultra low energy consumption. The scaling of devices has nevertheless helped to attain low power consumption, but still architectural improvements and power reduction techniques can further enhance the energy efficiency. The adiabatic logic is a proven technique to reduce dynamic power loss in digital systems. The energy loss is reduced as a large part of the charge supplied by the power supply is returned back to the supply instead of letting it flow to ground terminal [1]. The flow of energy in conventional CMOS logic is from supply to ground terminal through parasitic capacitances, where as in adiabatic logic, a major portion of the energy supplied by battery is returned back to the supply [2] as shown in Fig. 1. Another well established way of reducing power consumption is to make the system work in sub-threshold region by reducing the supply voltage below threshold level (V_{TH}) of a transistor. The sub-threshold system can attain reduction of power without sacrificing noise immunity and driving ability [3]. These two techniques can work in conjunction to attain ultra low power VLSI systems. The reduction in power is attained at the cost of maximum operation frequency of the logic. These systems typically work at a clock frequency ranging from a few hundreds of hertz to a few megahertz. The power consumption can be in range of few pico-watts. These systems are suitable for standalone operation where low power consumption is more important than the processing speed [4], biomedical application is one of such area which typically works at clock frequency below one MHz [5].

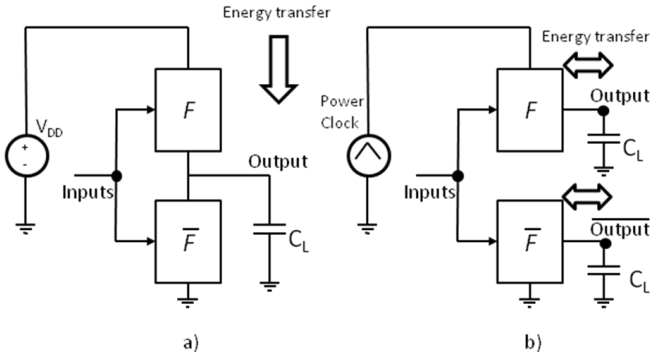


Fig. 1 The energy flow in a) conventional CMOS logic and b) Adiabatic logic.

The adiabatic circuits have many flavors like 2N2N2P [6], ECRL [7], PFAL [8] and SAL [3], they have shown promising results for better energy efficiency. These adiabatic circuits have latch based structure. The positive feedback in the latch ensures that system will attain either of the two stable states and avoid logic level degradation at the output nodes [9]. The loop gain of the latch also has impact on the energy losses; the energy losses are large when the latch is in intermediate stage.

The positive feedback also enhances properties like noise immunity and operating speed. The performance of the latch is dictated by its loop gain which is of the order of $(g_m r_o)^2$. The reduction in output impedance due to channel length modulation effect is a big concern for highly scaled devices [10]. This effect directly reduces the loop gain of the latch. The loop gain can be enhanced using cascoding of MOSFETs. The cascoding of MOSFETs also reduces the leakage current and further improves the efficiency [11]. Use of regular cascode may not be suitable in highly scaled devices, as the supply voltage available may be of order of twice V_{TH}. In paper [12] it is shown that self cascode technique can be used to obtain cascoding of transistors without reducing the swing. In self cascode technique two transistors are connected in series but one of them is *m* times wider than the other one, as shown in Fig. 2. In self cascode mode the wider transistor works in triode region and overall output resistance is increased by a factor of *m*. In this paper, we study the effect of using self cascode transistor in a latching component of a basic adiabatic circuit. We found the technique of using self cascode best suits the PFAL architecture and thus we call the combined structure as self-cascode positive feedback adiabatic logic (SC-PFAL) logic.

2. THEORY OF OPERATION

The idea is to build a library of logic gates with low power consumption. To achieve this, amalgamation of various low power strategies, which can gel together, were tested. In literature it is shown that the adiabatic logic circuit when used in sub-threshold region can reduce power consumption [3]. We in this paper are exploring effect of using the self cascoding structure in the sub-threshold adiabatic logic.

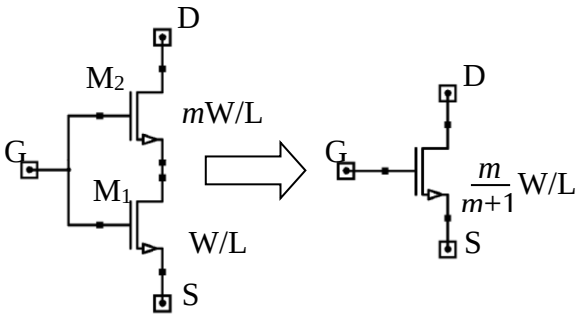


Fig. 2 Self Cascode Transistor.

The cascode logic as shown in Fig. 2, we have two series transistors with different width, which acts as equivalent to a single transistor [13]. The MOSFETs are in series and thus the currents in both of the transistors will be same. The two MOSFETs have same length but different widths thus the larger of the transistor will be in triode region and will have small drop across it, eventually in deep triode region the transistor M_2 will act like a small source degeneration resistor for M_1 [14]. This makes the self-cascode arrangement suitable for low voltage applications. The effective β of new transistor is not changed much as new β is given by equation 1 [15].

$$\beta_{eff} = \frac{\beta_1 \beta_2}{\beta_1 + \beta_2} \quad (1)$$

$$\text{if } \beta_2 = m.\beta_1 \quad (2)$$

$$\beta_{eff} = \frac{m}{m+1}\beta_1 \quad (3)$$

And if *m* is large β is almost equal to β_1 where as the small signal output resistance of the new cascode transistor is given by equation 4. The equation suggests the resistance is increased by a factor of intrinsic gain of transistor M_2; this can be seen in I_DV_D curves as shown in Fig. 3. The figure shows I_DV_D curve for both self cascode transistor and a normal NMOS transistor. It can be seen that the slope of self cascode structure is smaller that indicates increase in output resistance.

$$r_0 = (gm_2 r_2).r_1 - r_1 - r_2 \quad (4)$$

$$r_0 \approx (gm_2 r_2).r_1 \quad (5)$$

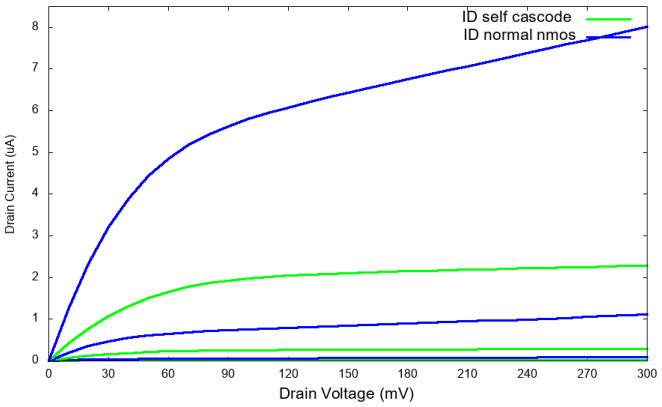


Fig. 3 I_DV_D graph to demonstrate increase in output impedance of a self cascode transistor in subthreshold region. The curves are plotted for gate potential of 0.1, 0.2 and 0.3 volts.

The overall gain of a self cascode inverter is given by equation 6 [17].

$$A = gm_1.r_1 + gm_2.r_2 + gm_1.gm_2.r_2.r_1 \quad (6)$$

The small signal output resistance is multiplied by intrinsic gain of the wider transistor. Thus, the self cascode transistor is able to provide higher output resistance without sacrificing much performance. The increase in r_0 of transistor will improve the performance of the latch as mentioned earlier. The loop gain of a latch is product of gain of individual inverter of the latch as shown in Fig. 4.

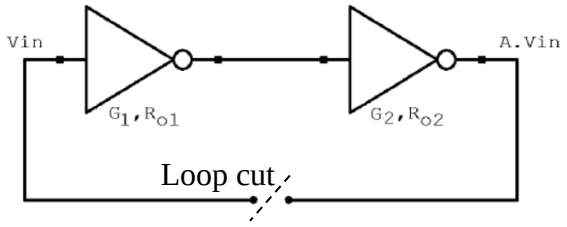


Fig. 4 Illustration of loop gain for a latch.

The loop gain is given by equation 7

$$A = (G_1 R_{01}).(G_2 R_{02}) \quad (7)$$

Improvement in R_0 will improve the loop gain in square proportion. One drawback of self-cascode transistor is it has a pole at lower frequency than the simple transistor and this makes the transition from high to low slower as time constant is increased as shown by equation 8 [15].

$$\tau_{selfcascode} = \tau_{simple}(1+\sqrt{1+m}) \quad (8)$$

The time constant degradation is not a concern, as in adiabatic circuits the power supply varies from low to high and no decision is made in adiabatic circuit while supply is high, also the operating frequency is low. Another advantage of cascoding is reduction in leakage power. This is significant as circuits operating in sub-threshold region operate at low frequencies and power consumed due to leakage current is a concern. The effective length of the cascode circuit increases with cascode parameter *m* and thus the leakage current is reduced. The advantage of using self cascode is reduction in area [15]. The total area occupied is less than the area of effective transistor.

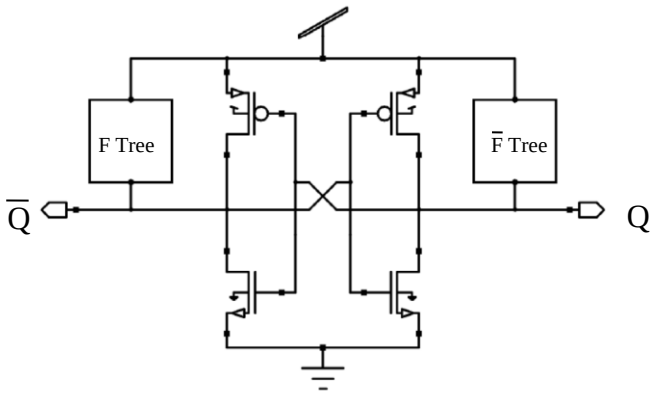


Fig. 5 Typical PFAL circuit.

Some standard adiabatic logic topologies like 2N2N2P, ECRL and PFAL [16] were simulated by replacing simple MOS transistors with self-cascode transistors in the latch. The PFAL topology was observed to provide better results. The PFAL adiabatic logic architecture contains a latch and two pull up network that realize a Boolean logic equation to be implemented as shown in Fig. 5.

3. PROPOSED SC-PFAL LOGIC FAMILY

A basic inverter in PFAL logic is chosen as a beginning point. A PFAL inverter with fanout of four is designed and simulated using 70nm model file provided by Predictive Technologies Model (PTM) [17]. The circuit is as shown in Fig. 6. The power supply is a triangular wave as shown in Fig.**14**.

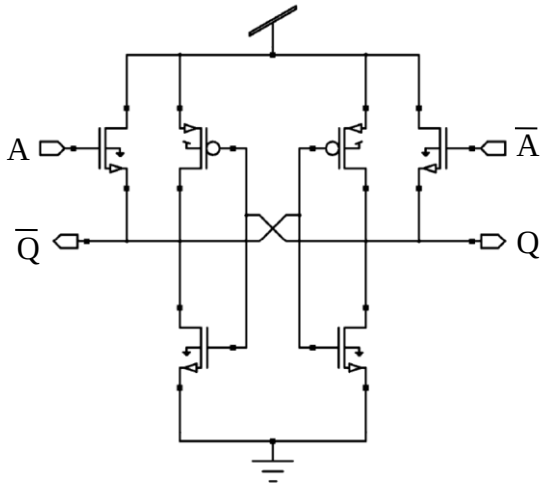


Fig. 6 PFAL inverter.

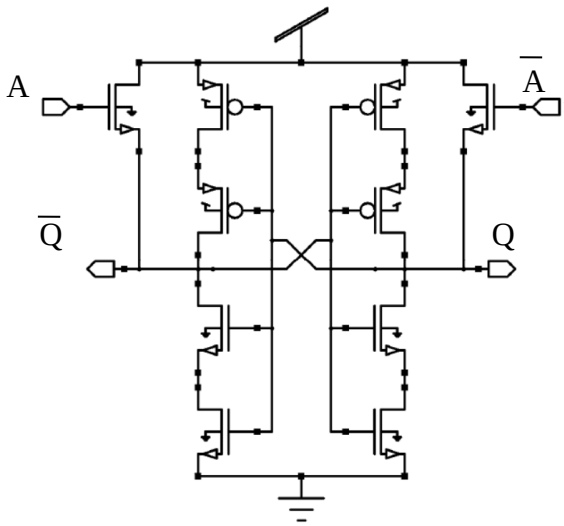


Fig. 7 SC-PFAL inverter.

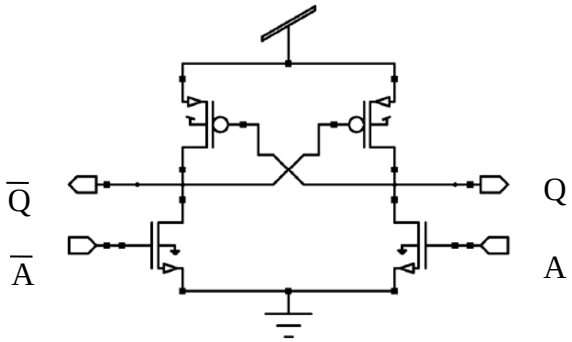


Fig. 8 ECRL inverter

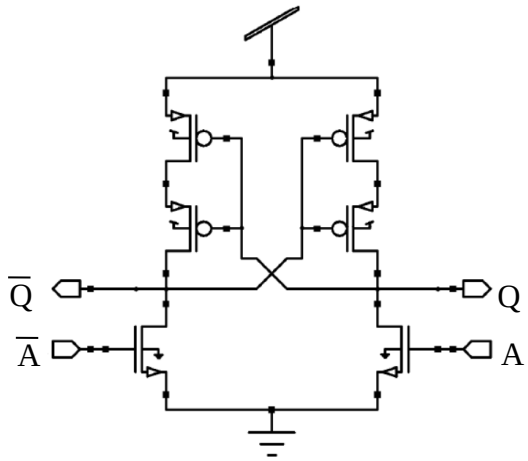


Fig.9 SC-ECRL inverter

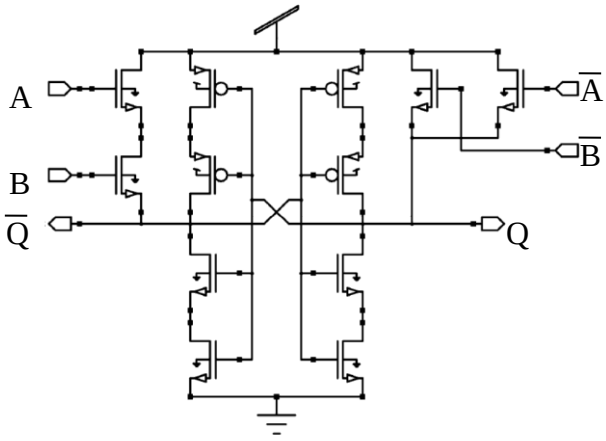


Fig.10 SC-PFAL two input NAND gate.

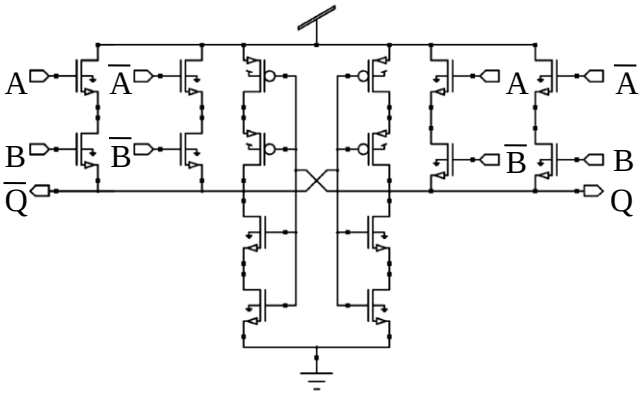


Fig.11 SC-PFAL XOR gate

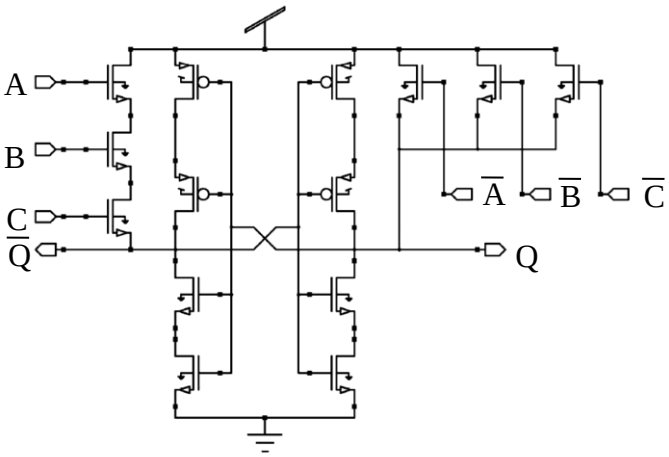


Fig.12 SC-PFAL three input NAND gate.

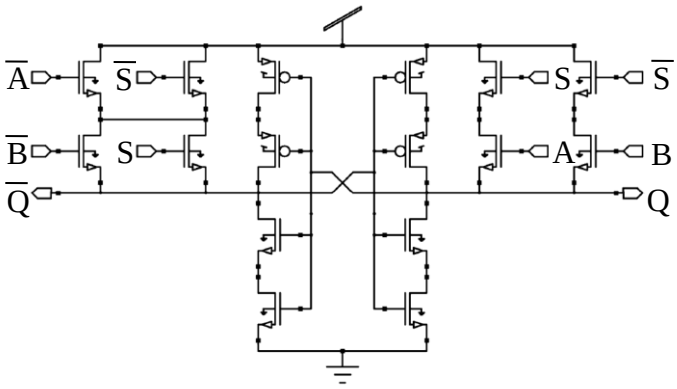


Fig.13 SC-PFAL multiplexer

The latch transistors of the PFAL circuit are then replaced with self cascode transistor as show in Fig. 7 to obtain SC-

PFAL inverter. To calculate the power consumption of the logic family a test bench is developed with a triangular wave voltage source as supply voltage and a load of four unit load (inverter) is placed at output of design under test. Similarly, other gates were designed and tested to develop a library. The library includes a two inputs NAND gate (

Fig.**10**), three inputs NAND gate (Fig.12), a two input XOR gate (

Fig.**11**), and a two to one multiplexer (Fig.13), using SC-PFAL logic.

4. SIMULATION RESULTS AND DISCUSSION

The circuit is designed using 70nm PTM model file with threshold voltages V_{thP} = -326mV and V_{thN} = 310mV and are simulated using T-Spice simulator. A 300mV triangular supply is used to power up the logic gates. The peak potential of 300mV of the supply ensures that the system remains in sub-threshold region during entire operation.

To evaluate the performance of proposed architecture, basic logic gates were designed and simulated. The results are tabulated in table 1. The plots are shown for simulations performed at a frequency of 250 kHz triangular wave at supply node.

TABLE 1
POWER CONSUMPTION OF VARIOUS GATES OF DIFFERENT FAMILIES (NW) WITH A SUPPLY VOLTAGE OF 0.3V TRIANGULAR WAVE AT 250KHZ.

Gate	PFAL	PFAL+SC*	ECRL	ECRL+SC*
Inverter	0.27	0.18	0.52	0.42
NAND2	0.49	0.43	0.57	0.52
NAND3	0.57	0.56	0.61	0.61
MUX(2:1)	0.93	0.71	0.82	0.72
XOR2	0.98	0.89	1.19	1.05

Simulation waveforms of a basic inverter is shown in Fig.**14**, and that of two input NAND gate and XOR gate is shown in Fig.15. The Fig.16 shows simulation waveform for a three input NAND gate and a 2:1 multiplexer.

The concept of self cascoding is also applied to ECRL logic as shown in Fig. 8 to evaluate the power consumption performance. The modified ECRL logic is shown in Fig.9. The table 1 shows that the adiabatic PFAL logic family responds better to self cascoding than adiabatic ECRL logic family. This can be justified as in PFAL logic family we have both PMOS and NMOS transistors in the latch network, whereas in ECRL logic family the positive feedback (latch) is comprised only of PMOS transistors.

It can be seen that the performance enhancement is better for gates like XOR and multiplexer where there exist multiple path from load capacitor to V_{DD}. The enhancement in power efficiency diminishes as path from load capacitor to V_{DD} has more transistors as in NAND gates. This leads to increase in resistance at charge recovery path and thus loss of energy. The best enhancement in power reduction is observed to be obtained for inverter. Statistics shows that inverters are most used logic gates in a typical logic circuit.

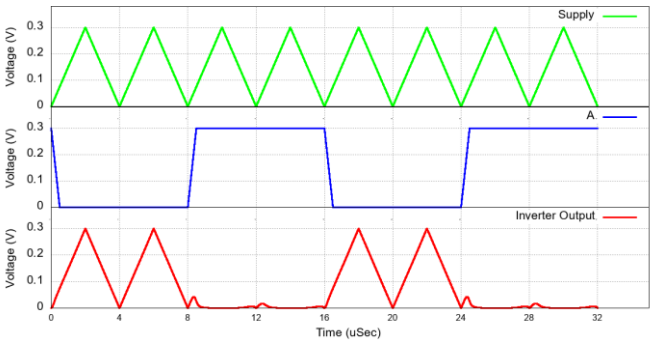


Fig.14 Input output waveform for an inverter of SC-PFAL family.

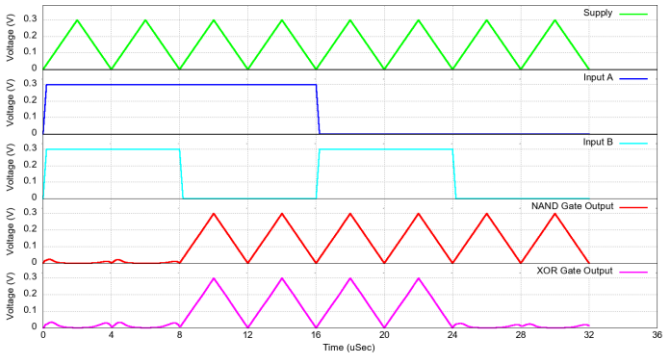


Fig.15 Input output waveform for a two input NAND gate and a two input XOR gate of SC-PFAL family.

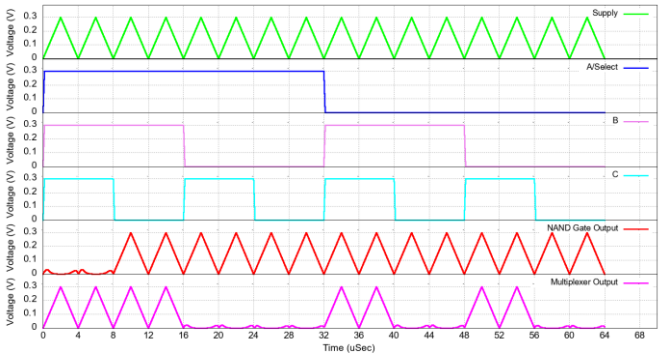


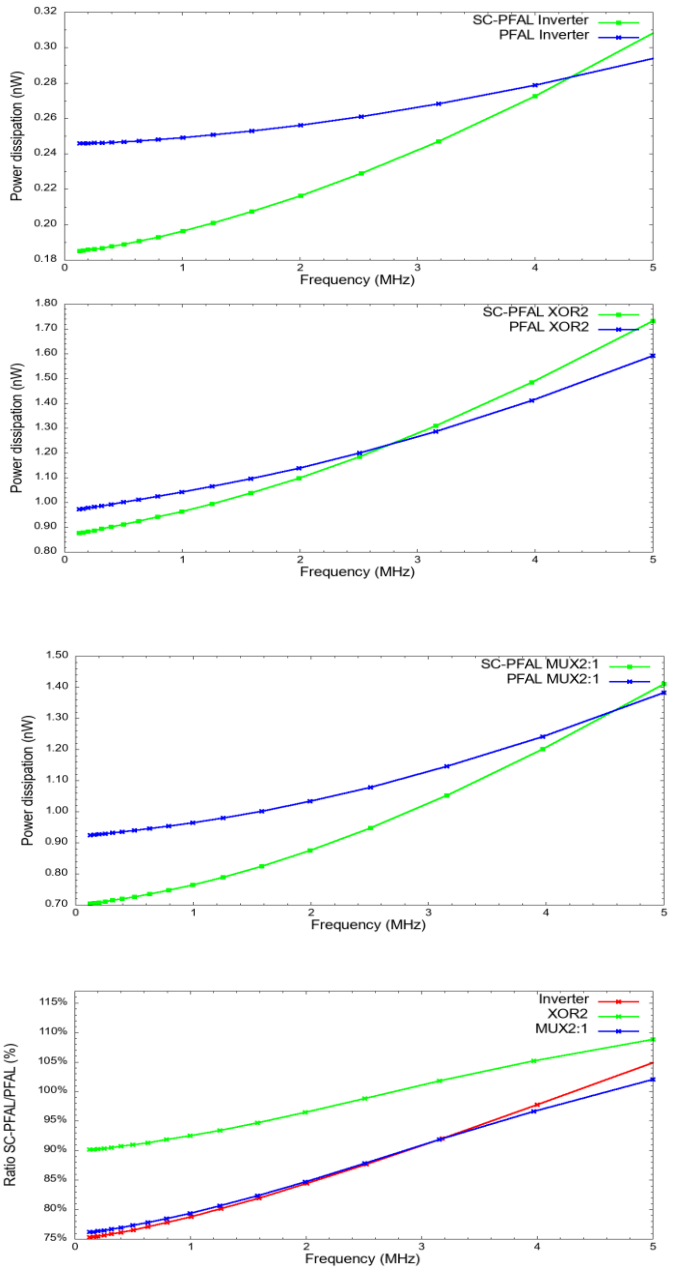
Fig.16 Input output waveform for a three input NAND gate and a Multiplexer of SC-PFAL family.

The enhancement in power efficiency of SC-PFAL inverter, two input XOR gate and a 2:1 multiplexer is compared with their PFAL counterparts in plots a), b) and c) of

Fig. 17 respectively. It is revealed that the SC-PFAL logic gives better results at lower frequencies. Plot d) in

Fig. 17 shows the power efficiency enhancement ratio (the ratio of power consumption of SC-PFAL gates to that of PFAL gates). Power efficiency enhancement ratio

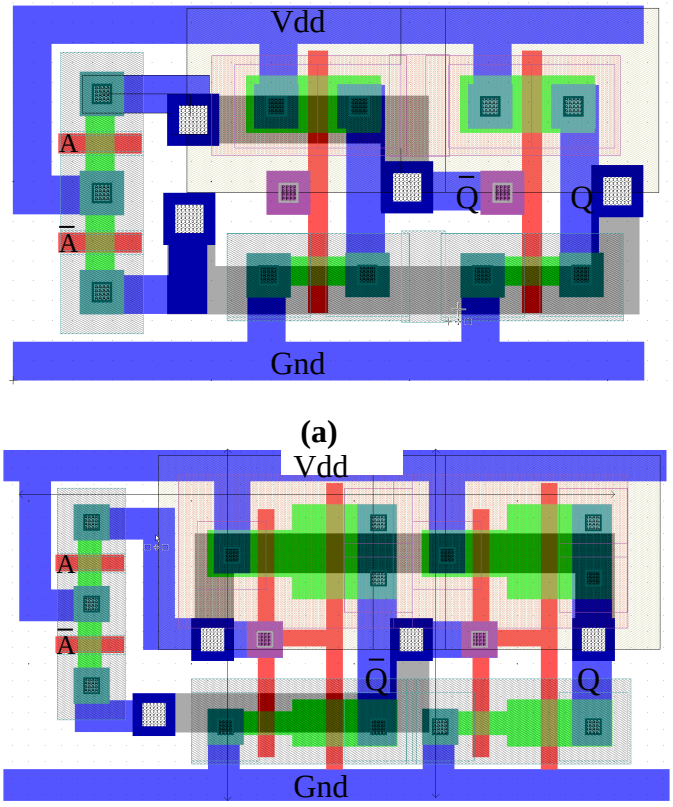
reaches approximately 75% asymptotically at very low clock frequencies for an inverter. The SC-PFAL logic has shown better energy efficiency than PFAL adiabatic logic up to 4MHz. The plot of power dissipation verses operating frequency shows that power efficiency performance of proposed circuit is better at lower operating frequency.



(d)

Fig. 17 Comparison of power dissipation of basic logic gates a) SC-PFAL inverter verses PFAL inverter, b) SC-PFAL two input XOR gate verses PFAL two input XOR gate, c) SC-PFAL 2:1 multiplexer verses PFAL 2:1 multiplexer, d) plots of ratio of power consumption for SC-PFAL to that of PFAL gates.

Addition of extra transistors increases the footprint area of the logic gate. To access the impact of increase in area of the gate a layout of the proposed inverter and a basic PFAL inverter is created. The MOSFETs used are predictive technology models and thus tool kit is not available so the layout is designed using a standard tool kit available with Tanner EDA. The layout of PFAL inverter and a proposed inverter is shown in Fig. 18 a) and b) respectively.



(a)

(b)

Fig. 18 Layout of (a) SC-PFAL inverter and (b) PFAL inverter

The area of a PFAL inverter is 38.0 μm^2 where as the area of proposed SC-PFAL inverter is 49.4 μm^2. The area overhead is thus 30% of the PFAL inverter area.

5. CONCLUSION

A modified PFAL logic self cascode PFAL logic is proposed that is having better efficiency at lower operating frequencies in sub-threshold region. To reduce the power consumption the concept of self cascoding is applied to the latch present in adiabatic PFAL logic and ECRL logic. The effect of self cascoding on various logic gates were explored for both PFAL and ECRL logic. The simulations results show that PFAL logic is better suited for applying self cascode transistors. The power consumption of proposed SC-PFAL inverter is 25% less than its counterpart PFAL logic at near DC frequencies of power clock of adiabatic circuit. The power efficiency is improved at the cost of area which is increased by 30%. The summary is the SC-PFAL logic can prove a good building block for systems operating at very low power regime.

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